ABSTRACT OF THE DISCLOSURE

In a method for forming a via hole of a semiconductor device, a first step via hole is formed in a SiO_2 layer/etching-step layer/Cu layer laminate, this formation being stopped at the etching-stop layer, after which resist is peeled away, and a second step via hole continuous with the first step via hole is formed in the etching-stop layer. These via holes are patterned and a barrier film is formed thereonto using sputtering. By shortening the overetching time an increase in the electrical resistance of the Cu-Cu connection is suppressed, and current leakage is prevented.